HIGHLY EFFICIENT COMPACT Q-BAND MMIC POWER AMPLIFIER USING 2-MIL SUBSTRATE AND PARTIALLY-MATCHED OUTPUT

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ABSTRACT

Presented is an 850 mW Q-Band PHEMT MMIC power amplifier with a peak efficiency of 34% at 45.5 GHz, believed to be the highest reported at this power level and frequency. The compact amplifier (3.6 mm by 1.6 mm) features the use of a thinned 2-mil GaAs substrate and off-chip output matching and combining on a 5-mil alumina substrate.

INTRODUCTION

High efficiency Q-band power amplifiers are a necessity for many EHF SATCOM ground terminal applications. Previous work has demonstrated high power and power-added efficiency single-chip HEMT MMIC performance using 4-mil substrate [1], 2-mil substrate [2], 4-mil InP substrate [3], as well as single and dual-stage MIC amplifiers using discrete 2-mil HEMT devices [4]. This work improves the state-of-the art performance with a peak output power of 850 mW with 11.3 dB gain and 34% PAE. The amplifier is also very compact, measuring 3.6 mm by 1.6 mm. The narrow chip width makes the chip ideal for transmit phased array applications where the frequency limits antenna element spacings. The small chip size also means more chips can be fabricated on a single wafer, leading to lower cost transmitters.

POWER AMPLIFIER DESIGN

The MMIC power amplifier was designed for fabrication using TRW's pseudomorphic InGaAs 0.15 μm T-gate power HEMT process

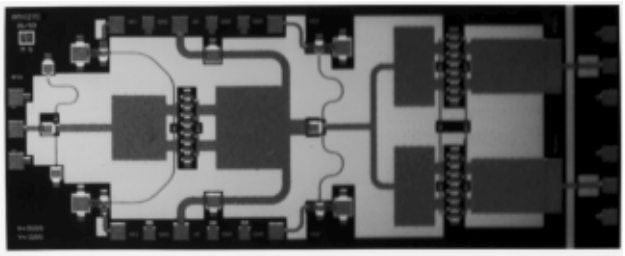

Figure 1. 2-Mil Thick MMIC Power Amplifier.

with some key modifications from the previously reported process [5,6]. First, the 0.15 μm gate length pseudomorphic AlGaAs/$In_{0.22}Ga_{0.78}As$/GaAs HEMT device has been optimized to achieve the highest power added efficiency, power density and gain at Q-band. The second addition is a thin 750Å PECVD silicon nitride passivation for the PHEMT device to minimized device feedback capacitance and other parasitic capacitances. After the top side MMIC processing is completed, the wafers are thinned to 2 mils, rather than our standard 4 mils. This allows us to etch smaller via holes and to place via holes for every source pad of the FET devices. Because of the thinner substrate and more frequent via holes, the device source inductance is greatly reduced as well as the thermal resistance of the device. These factors greatly help in the gain, power density, and efficiency of the MMICs.

The amplifier is a 2-stage design, with 0.8 mm of device periphery in the first stage driving 2 mm in the second stage. The input is matched to a standard 50 ohm impedance, using what is essentially a low-pass matching structure. Gate bias for the first and second stages as well as the first stage drain bias are provided by pads on either side of the chip and contain on-chip bias networks of thin film

resistors and MIM capacitors to provide stability. The output of the amplifier is 2 ports (after an interstage power split), each with 1 mm of device periphery. The 2 ports are matched to a real 36 ohm impedance level, to be combined and transformed by the off-chip combiner. The drain bias for the output stages is also provided through the combiner network. By moving the final combining and matching structures and the 2nd stage biasing off-chip, the MMIC size has been greatly reduced and the overall performance of the amplifier improved because of the lower loss alumina substrate. Figure 1 is a photo showing the completed MMIC power amplifier. The circuit output ports include extra lengths of 50 ohm line and pads for on-wafer measurement with standard 200 μm pitch GSG RF probes. This output section gets chopped off when the circuit is mounted for fixture test.

OFF-CHIP COMBINER DESIGN

The off-chip combiner (Figure 2) takes two 36 ohm signals, combines them, and then transforms them to 50 ohms by means of a quarter-wave transformer. The combiner is a fairly standard Wilkinson, but designed for 36 ohm impedances rather than 50 ohm. The combiner is implemented on 5-mil alumina substrate and also includes dual-sided bias connections for the drain of the second stage devices by means of an RF choke implementedwith microstrip radial stubs.

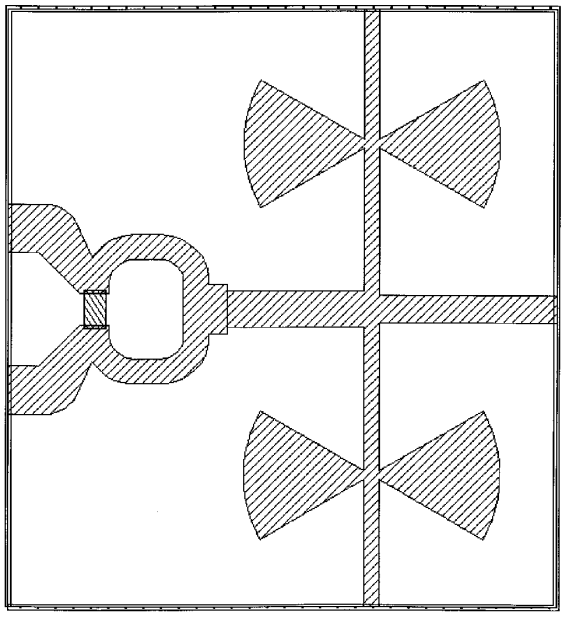

Figure 2. 2-Way 36 Ohm Wilkinson Combiner.

MEASURED RESULTS

Figure 3 shows the fixtured power amplfier configuration, as measured with waveguide. A 5 mil quartz input substrate feeds the RF signal to the chip, and the 5 mil alumina substrate performs the output combining. The amplifier was tested in a waveguide environment using finline-to-microstrip transitions on the input and output ports. The DC bias connections are also shown, with shunt 100 pF chip capacitors on each line to provide additional bypassing. The second stage drain bias connection is out of view to the right in the picture, injected through the alumina substrate.

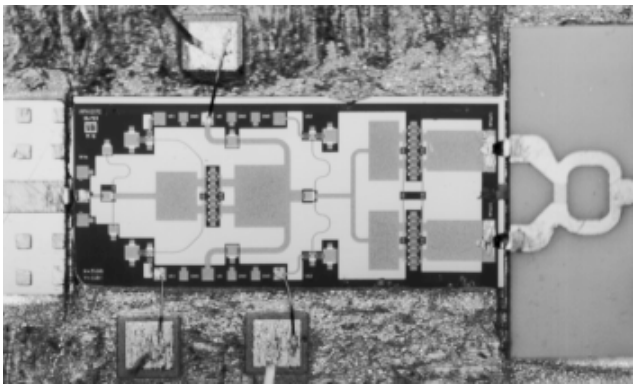

Figure 3. Fixtured Power Amplifier.

The measured results versus input power are plotted in Figure 4 for an input frequency of 45.5 GHz. The amplifier efficiency peaks at 33.8% at an input power of 18 dBm with an output power of 29.25 dBm. The performance over frequency is shown in Figure 5 for an input power of 18 dBm. The PAE peaks again at 33.8% at 45.5 GHz and the output power at that point is 29.3 dBm (850 mW). The minimum efficiency and power of a 2 GHz band from 44 to 46 GHz are 31% and 28.8 dBm, respectively. The measured data is referenced to a 50 ohm microstrip impedance at the input of the quartz substrate and the output of the alumina substrate, so the loss of the input 50

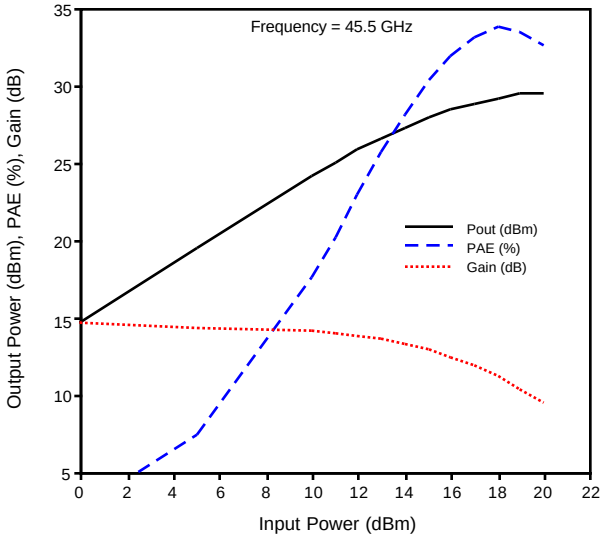

Figure 4. Performance vs. Input Power.

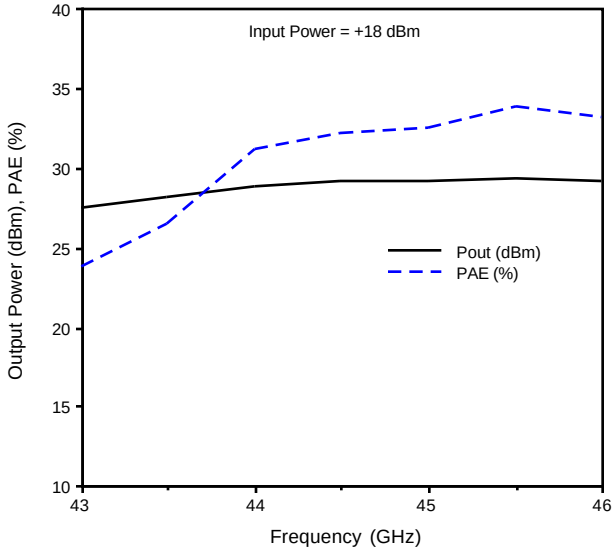

Figure 5. Performance vs. Frequency.

ohm substrate and the output combiner are included.

CONCLUSION

We have demonstrated a highly efficient MMIC power amplifier using a 2-mil thick PHEMT MMIC process. The amplifier delivers what we believe to be the best power-added efficiency reported to date at Q-Band frequencies and watt-level output powers, a peak of 34% at 45.5 GHz. The amplifier delivers 850 mW of output power and 11.3 dB of gain at this operating point.

ACKNOWLEDGEMENTS

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